

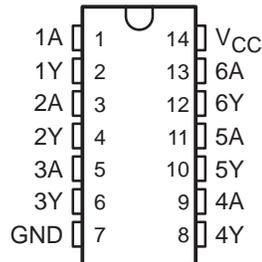
SN54AC14, SN74AC14 HEX SCHMITT-TRIGGER INVERTERS

SCAS522F – AUGUST 1995 – REVISED OCTOBER 2003

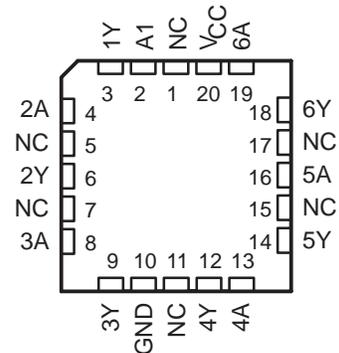
- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 9.5 ns at 5 V

SN54AC14 ... J OR W PACKAGE
SN74AC14 ... D, DB, N, NS, OR PW PACKAGE

(TOP VIEW)



SN54AC14 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \bar{A}$. Because of the Schmitt action, they have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. They also have a greater noise margin than conventional inverters.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AC14N	SN74AC14N
	SOIC – D	Tube	SN74AC14D	AC14
		Tape and reel	SN74AC14DR	
	SOP – NS	Tape and reel	SN74AC14NSR	AC14
	SSOP – DB	Tape and reel	SN74AC14DBR	AC14
	TSSOP – PW	Tube	SN74AC14PW	AC14
		Tape and reel	SN74AC14PWR	
-55°C to 125°C	CDIP – J	Tube	SNJ54AC14J	SNJ54AC14J
	CFP – W	Tube	SNJ54AC14W	SNJ54AC14W
	LCCC – FK	Tube	SNJ54AC14FK	SNJ54AC14FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54AC14		SN74AC14		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	6	2	6	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V		-12	-12	mA
		$V_{CC} = 4.5$ V		-24	-24	
		$V_{CC} = 5.5$ V		-24	-24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	12	mA
		$V_{CC} = 4.5$ V		24	24	
		$V_{CC} = 5.5$ V		24	24	
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SCAS522F – AUGUST 1995 – REVISED OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AC14		SN74AC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{T+} Positive-going threshold		3 V	0.8	1.8	2.2	0.8	2.2	0.8	2.2	V
		4.5 V	1.5	2.6	3.2	1.5	3.2	1.5	3.2	
		5.5 V	1.6	3.2	3.9	1.6	3.9	1.6	3.9	
V _{T-} Negative-going threshold		3 V	0.5	0.8	1	0.5	1	0.5	1	V
		4.5 V	0.9	1.4	1.8	0.9	1.8	0.9	1.8	
		5.5 V	1.1	1.8	2.3	1.1	2.3	1.1	2.3	
ΔV _T Hysteresis (V _{T+} - V _{T-})		3 V	0.3	1	1.2	0.3	1.2	0.3	1.2	V
		4.5 V	0.4	1.2	1.4	0.4	1.4	0.4	1.4	
		5.5 V	0.5	1.4	1.6	0.5	1.6	0.5	1.6	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -12 mA	3 V	2.56			2.4		2.48		
		4.5 V	3.86			3.7		3.8		
	I _{OH} = -24 mA	4.5 V	3.86			3.7		3.8		
		5.5 V	4.86			4.7		4.8		
I _{OH} = -50 mA [†]	5.5 V				3.85					
I _{OH} = -75 mA [†]	5.5 V						3.85			
V _{OL}	I _{OL} = 50 μA	3 V	0.002		0.1	0.1		0.1		V
		4.5 V	0.001		0.1	0.1		0.1		
		5.5 V	0.001		0.1	0.1		0.1		
	I _{OL} = 12 mA	3 V				0.36		0.5		
		4.5 V				0.36		0.5		
	I _{OL} = 24 mA	4.5 V				0.36		0.5		
		5.5 V				0.36		0.5		
I _{OL} = 50 mA [†]	5.5 V						1.65			
I _{OL} = 75 mA [†]	5.5 V						1.65			
I _I	V _I = V _{CC} or GND	5.5 V	±0.1			±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	2			40		20		μA
C _i	V _I = V _{CC} or GND	5 V	4.5							pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			SN54AC14		SN74AC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1.5	6	13.5	1	16	1.5	15	ns
t _{PHL}			1.5	6	11.5	1	14	1.5	13	



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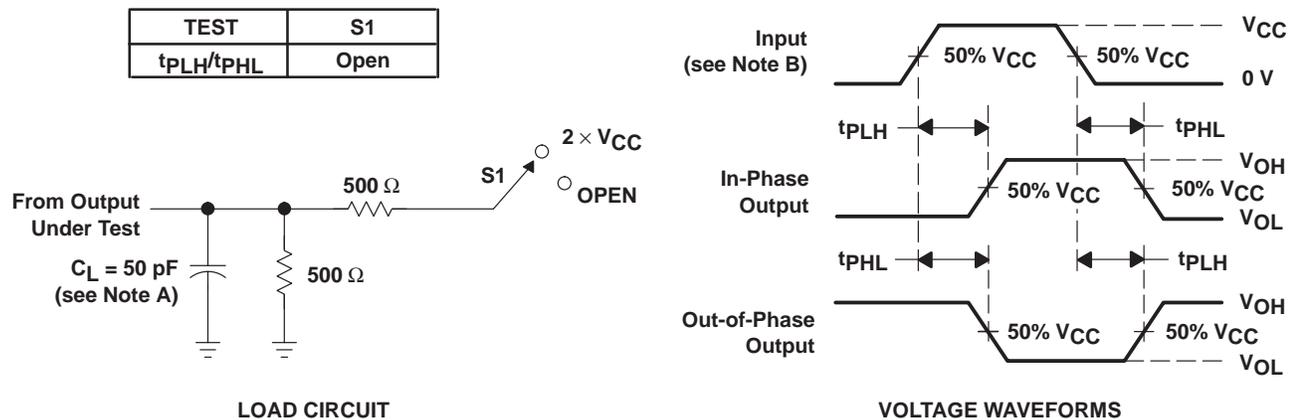
switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC14		SN74AC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	5	10	1.5	12	1.5	11	ns
t_{PHL}			1.5	5	8.5	1.5	10	1.5	9.5	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	25	pF

PARAMETER MEASUREMENT INFORMATION



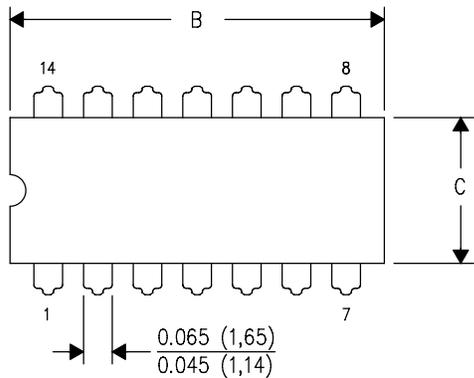
- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

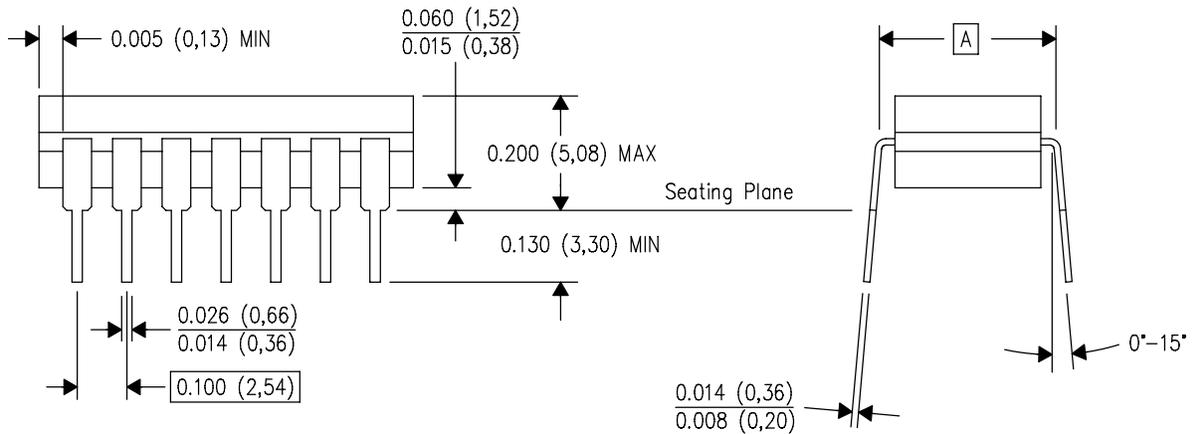
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

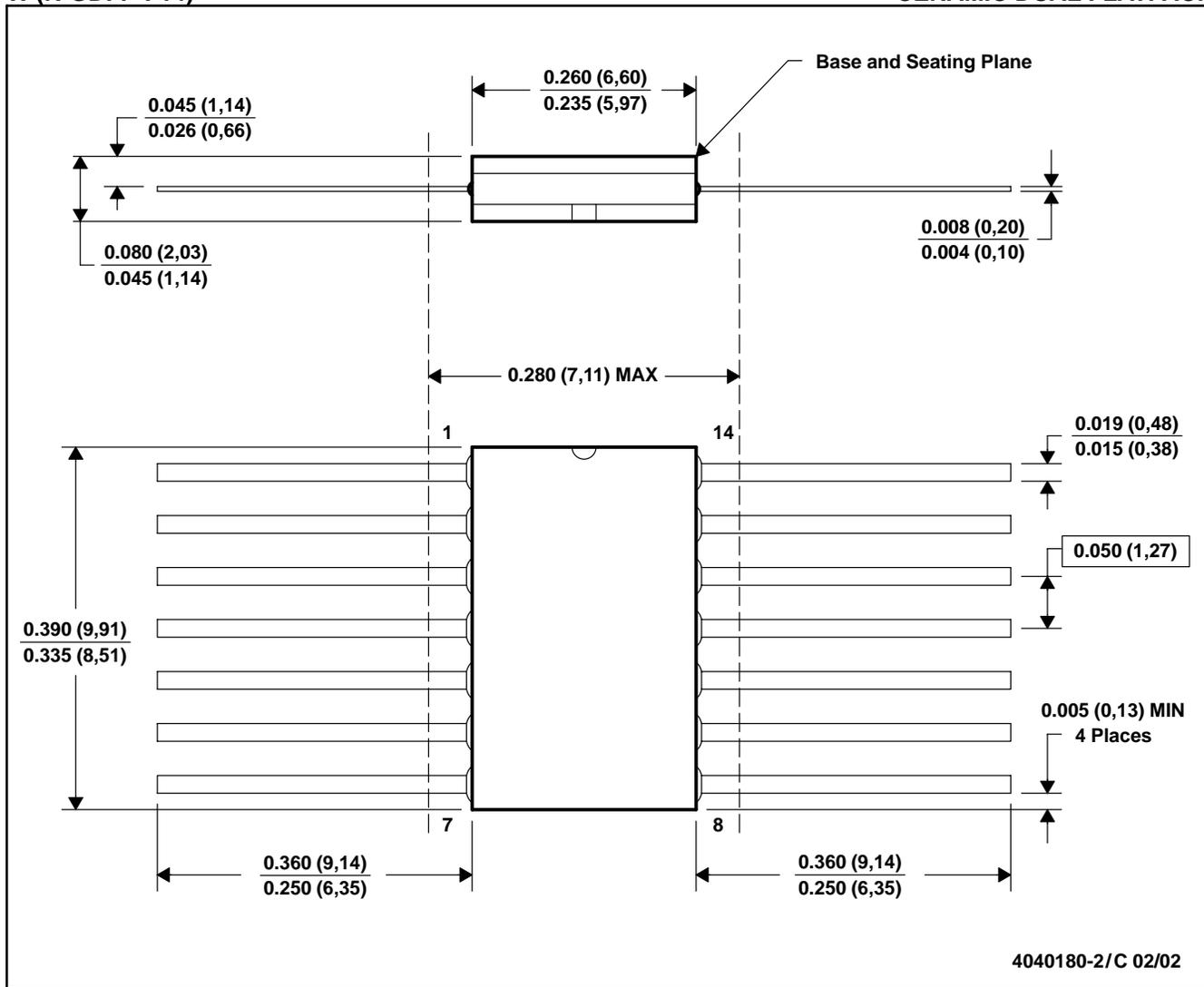


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

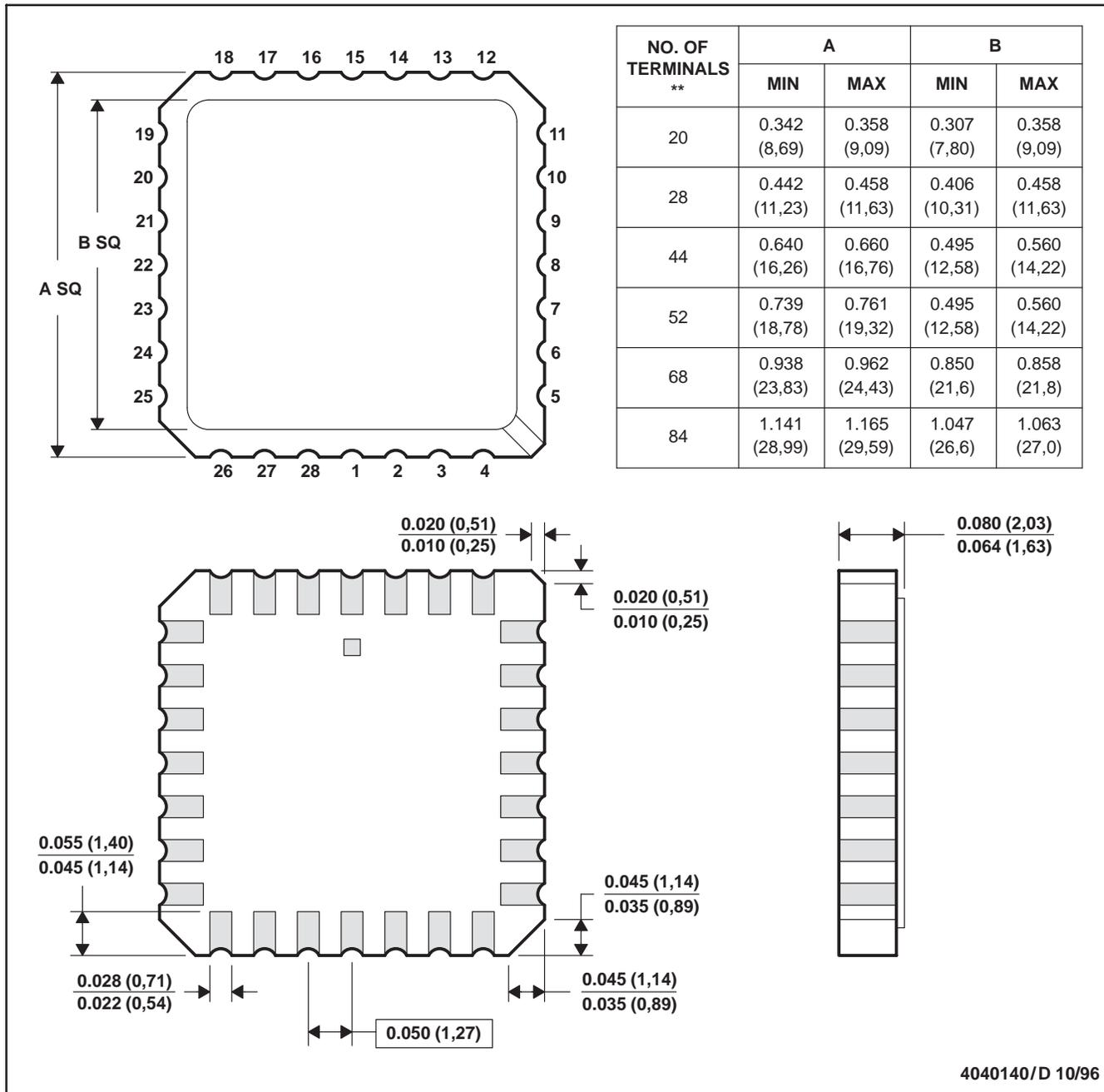


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

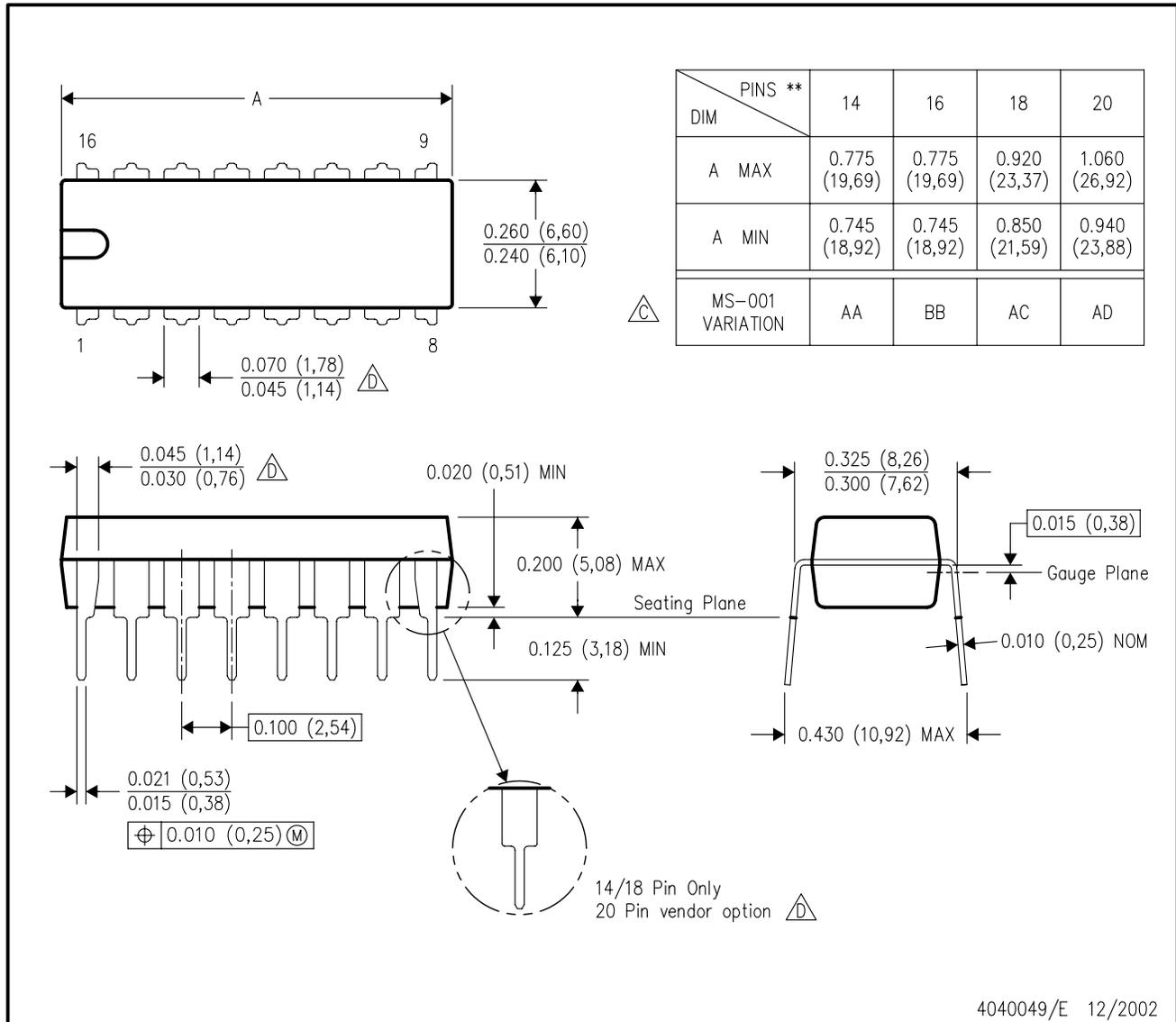


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

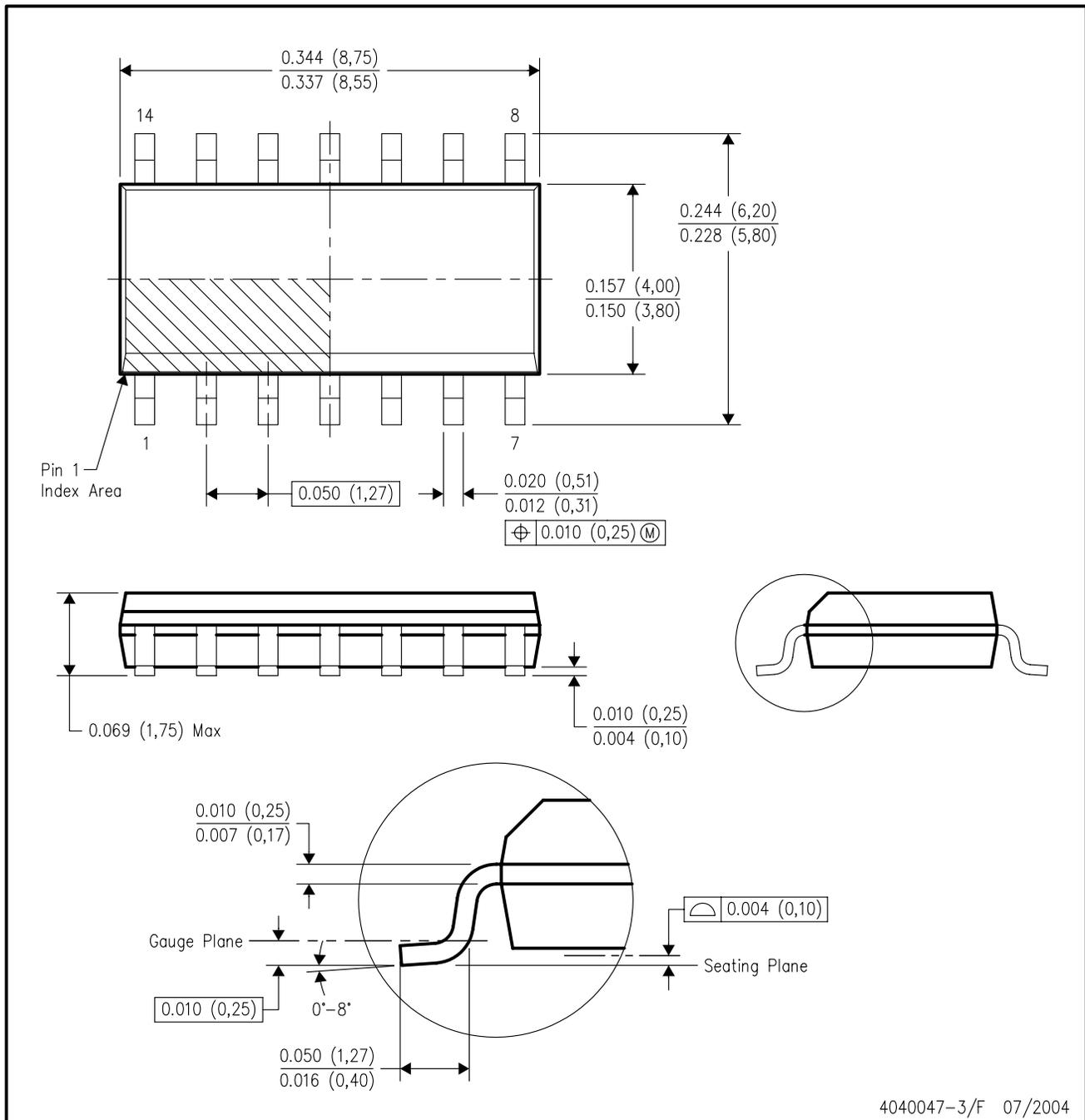


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



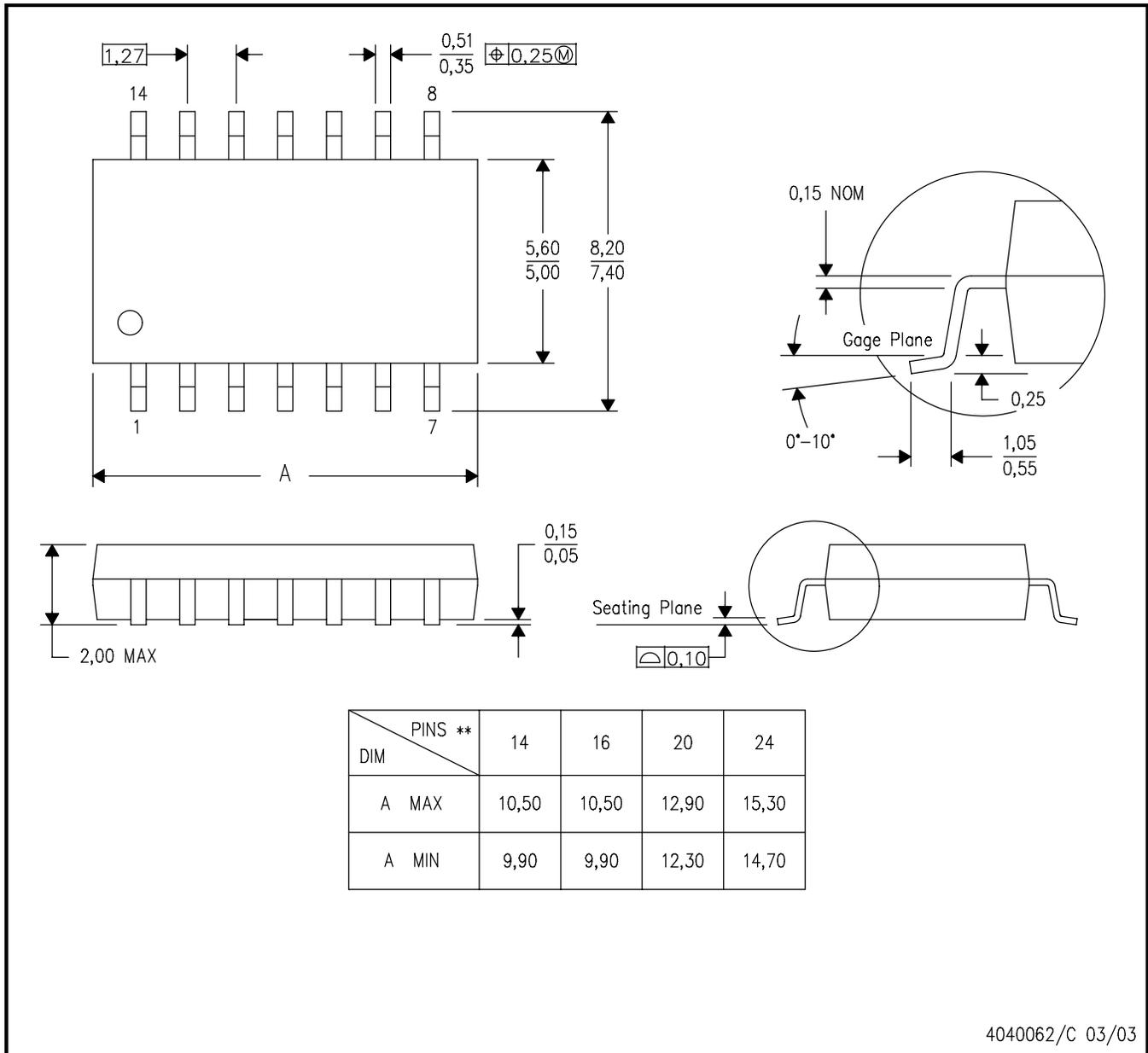
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

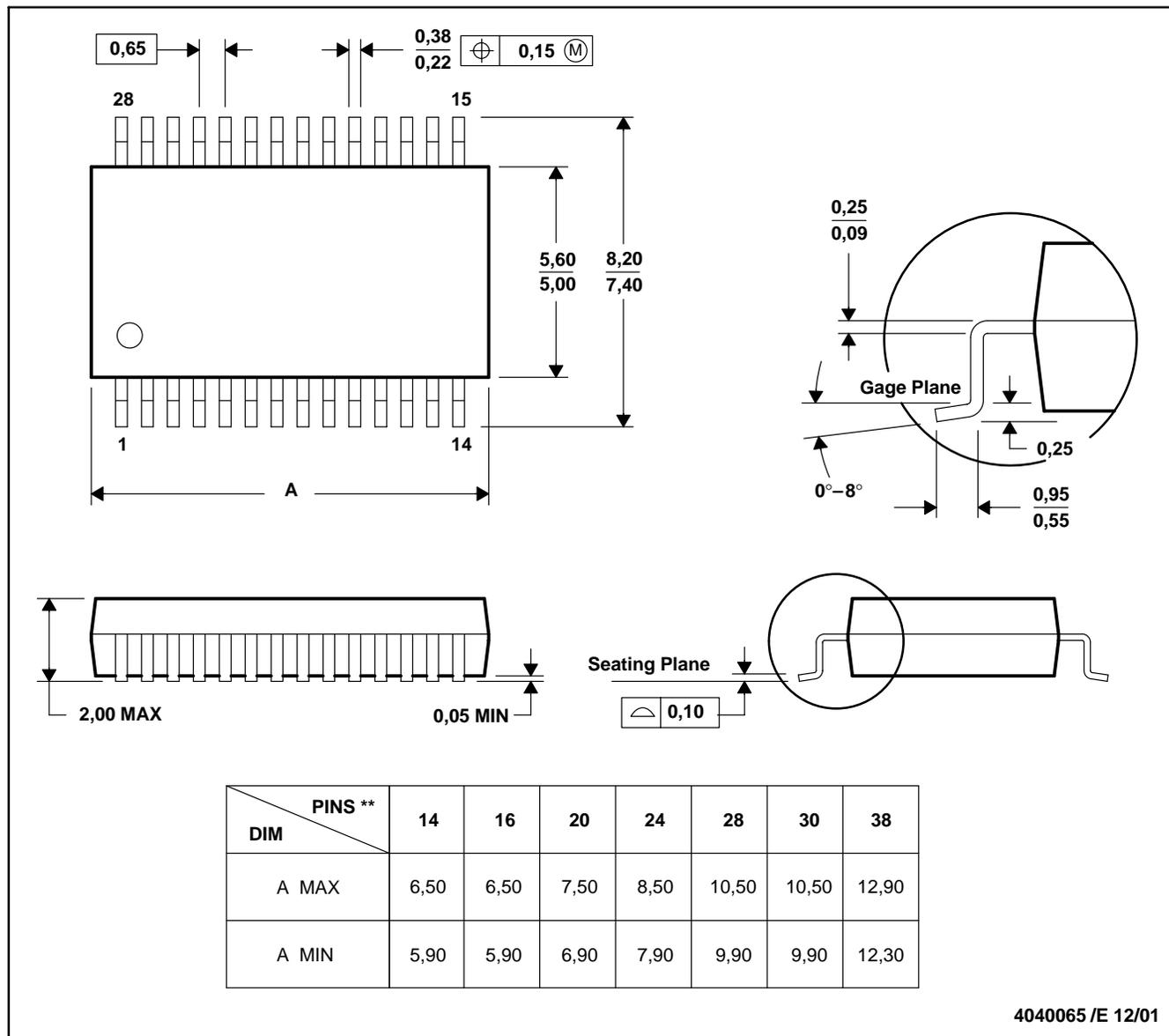


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

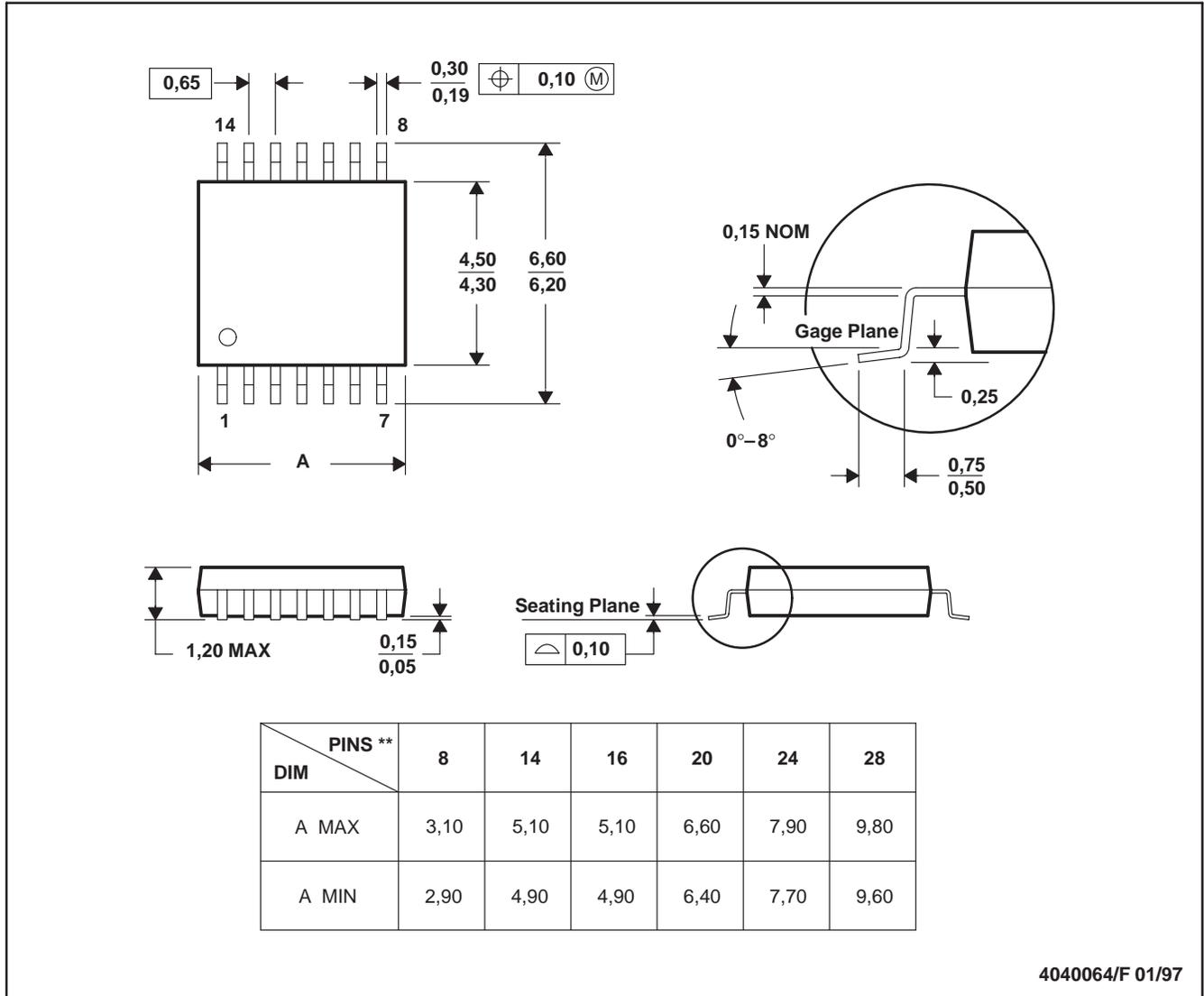


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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